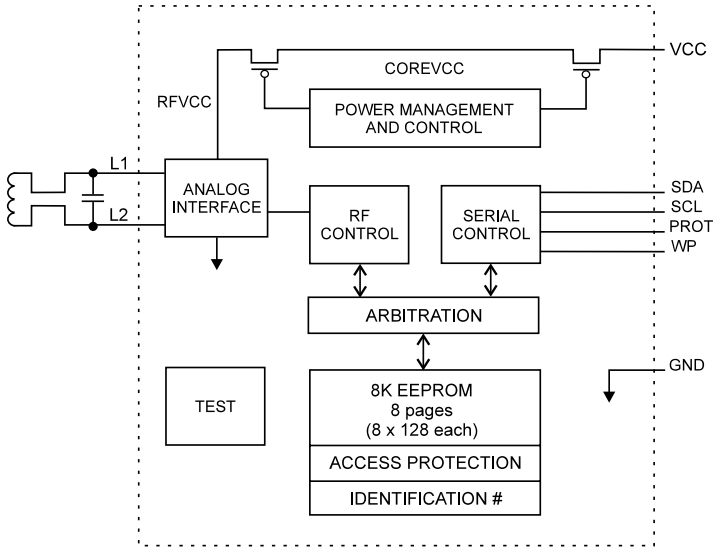
Features

- **Dual-port Nonvolatile Memory - RFID and Serial Interfaces**
- **Two-wire Serial Interface:**
  - **Compatible with a Standard AT24C08 Serial EEPROM**
  - **Programmable Access Protection to Limit Reads or Writes from Either Port**
  - **Lock/Unlock Function, Coil Connection Detection**
- **RFID Interface:**
  - **125 kHz Carrier Frequency for Long Range Access**
  - **2-Wire Connection to External Coil Antenna and Tuning Capacitor**
  - **Multi-tag Management to Handle Several Tags in the Field at Once**
  - **12 RFID Commands for Tag Control and Memory Read/Write**
  - **ID Write and Lock from RFID Port**
  - **Ultra Low Power Single Bit Write - 25 µA**
- **Highly-reliable EEPROM Memory**
  - **8K bits (1K bytes), Organized as 8 Blocks of 128 Bytes Each**
  - **16-byte Page Write, 10 ms Write Time**
  - **10 Years Retention, 100K Write Cycle Endurance**
- **-40°C to +85°C Operation, 2.4V to 5.5V Supply, 8-Lead JEDEC SOIC Package**

Description

The AT24RF08C functions as a dual access EEPROM, with both a wired serial port and a wireless RFID port used to access the memory. Access permissions are set from the serial interface side to isolate blocks of memory from improper access. The RFID interface can be powered solely from the attached coil permitting remote reads and writes of the device when VCC is not applied.

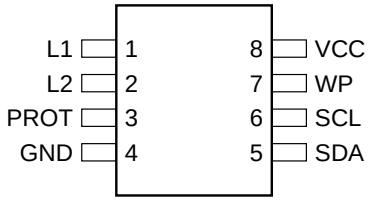
Block Diagram



Pin Configurations

Pin Name	Function
L1	Coil Connection
L2	Coil Connection
PROT	Protection Input
GND	Ground
SDA	Serial Data,Open Drain I/O
SCL	Serial Clock Input
WP	Write Protect Input
VCC	Supply: 2.4V - 5.5V

8-Pin SOIC



Asset Identification EEPROM

AT24RF08C

Rev. 1072E–09/99

General Overview

The AT24RF08C is intended to be pin compatible with standard serial EEPROM devices except for pins 1, 2 and 3, which are address pins in the standard part. Other exceptions to the AT24C08 Serial EEPROM data sheet are noted in the “Serial EEPROM Exceptions” section later in this document. Connection of an external coil antenna and optional tuning capacitor, normally via a two conductor wire, is all that is required to complete the RFID hardware requirements.

Throughout this document, the term “reader” is defined as the base station that communicates with the chip. Under all expected conditions, it actually serves as both a reader and writer. The term ‘tag’ is used to indicate the chip when operating as an RFID transponder with the coil attached.

All bits are sent to or read from the device, most significant bit first, in a manner consistent with the AT24C08 Serial EEPROM. The bit fields in this document are correspondingly listed with the MSB on the left and the LSB on the right.

EEPROM Organization

The EEPROM memory is broken up into 8 **blocks** of 1K bits (128 bytes) each. Within each block, the memory is physically organized into 8 **pages** of 128 bits (16 bytes) each. In some instances, accesses take place on a 32-bit (4 byte) **word** basis. In addition to these 8K bits, there are two more 128-bit pages that are used to store the access protection and ID information. There are a total of 8448 bits of EEPROM memory available on the AT24RF08C.

Access protection (both read and write) is organized on a block basis for blocks 1 through 7 and on a page and block basis for block 0. Protection information for these blocks and pages is stored in one of the additional pages of EEPROM memory that is addressed separately from the main data storage array. See “Access Protection” on page 3 for more details.

The ID value (see “ID Configuration” on page 7) is located in the ID page of the EEPROM, the second of the additional 16 byte pages.

Writes from the serial port may include from one to 16 bytes at a time, depending on the protocol followed by the bus master. Accesses to the EEPROM from the RFID port are on either a word (32 bits) or page (128 bits) basis only. All page accesses must be properly aligned to the internal EEPROM page.

The EEPROM memory offers an endurance of 100,000 write cycles per byte, with 10 year data retention. Writes to the EEPROM and tamper bit take less than 10 ms to complete.

Completion time for writes initiated from the RFID port are different depending on the situation. When external power is supplied to the chip through the VCC pin, writes to the EEPROM and tamper bit take less than 11.8 ms when measured from the last modulation edge before the write to the first after the write. When powered from the coil pins at 125 KHz, the EEPROM write time will be 5.8 ms and the tamper write time will be 7.9 ms.

After manufacturing, all EEPROM bits except in the device revision byte (see “Access Protection” page 5) will be set to a value of 1 and the tamper bit will be set to 0.

Device Access

The third device address bit in the two wire protocol that is usually matched to A_2 (pin 3) on a standard AT24C08 serial EEPROM is internally connected high, so device addresses A8 through AF (hex) are used to access the memory on the chip. The general command encoding used by the serial port for EEPROM accesses is shown below in Device Access Examples, where $B_{2\text{-}0}$ is the block number, $P_{2\text{-}0}$ is the page number within the block and $A_{3\text{-}0}$ is the byte address within the page. Bits denoted as “x” are ignored by the device.

The PROT pin is used as a power good signal. When this pin is low, the serial port is held in reset and all sticky bits are set to one. When high, activity on the serial bus is permitted.

Device Access Examples

For Write Operations:

1 0 1 0 1 B_2 B_1 0 B_0 P_2 P_1 P_0 A_3 A_2 A_1 A_0 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0 …

For Read Operations:

1 0 1 0 1 X X 1 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0 …

Access Protection

All access protection bits are stored on a separate page of the EEPROM that is not accessed using the normal commands of an AT24C08 memory. See the “Access Protection Page” section on page 5, for more detail on this information.

The RFID Access (RF) fields in the Access Protection Page determines whether or not the corresponding block within the memory can be read or written via the RFID interface. If an illegal command is attempted, the command will be aborted. The MSB, if clear, prohibits all accesses from the RFID port, and the LSB if clear prohibits writes from the RFID port. The fields are stored in the EEPROM and organized as follows:

RFID Access Fields (RF)

MSB	LSB	Function
0	0	No accesses permitted from RFID port
0	1	No accesses permitted from RFID port
1	0	Reads only from the RFID port
1	1	No restrictions for RFID accesses

The Protection Bits (PB) fields in the Access Protection Page determine what type of accesses will be permitted via the serial port for each of the blocks on the chip. If an illegal access is attempted, the command will be NACK’ed. The MSB, if clear, prohibits all accesses to the block, and the LSB if clear prohibits writes. The fields are stored in the EEPROM and are organized as follows:

Protection Bits (PB)

MSB	LSB	Function
0	0	No accesses permitted in the block
0	1	No accesses permitted in the block
1	0	Read only, writes cause a NACK
1	1	Read/write - No access constraints for data within this block

The Tamper Write (TW) bits within the access protection page control whether or not a write will be permitted into the corresponding block of memory when the Tamper Bit is set. If the Tamper Bit is a 1 and the TW bit is a 0, then writes to that block from the RFID port are not permitted. In all other cases, writes are permitted according to the RF field value for that block. The value of this bit does not affect accesses from the serial port.

Accessed within the Access Protection Page is an individual CMOS Sticky Bit (SB) for each of the 8 blocks on the device. When the value of the sticky bit is 0, the Protection Bits (PB) for the corresponding block may not be changed via the software. These bits are all set to one when power is initially applied or when the PROT pin is low. These sticky bits may be written only to a 0 via the serial interface using the standard serial write operations. Reading the sticky bits does not affect their state.

Because access permissions are set individually for each of the blocks, all reads via the serial port will only read bytes within the block that was specified when the current address was latched into the device (with a write command). The block address bits (B_2 or B_1) that are sent with the write command are ignored on a read command.

After the read of the last byte within a block, the internal serial address wraps around to point at the beginning of that block. After the write of the last byte in a page, the internal address is wrapped around to point to the beginning of that page. If more than 16 bytes are sent to the device with a write command, the data written to any overlapping bytes will be corrupted.

If the WP pin is high, all write operations are prohibited from the serial port, although write commands may be used to set the address for a subsequent read command.

Block 0 Write Protection Bits

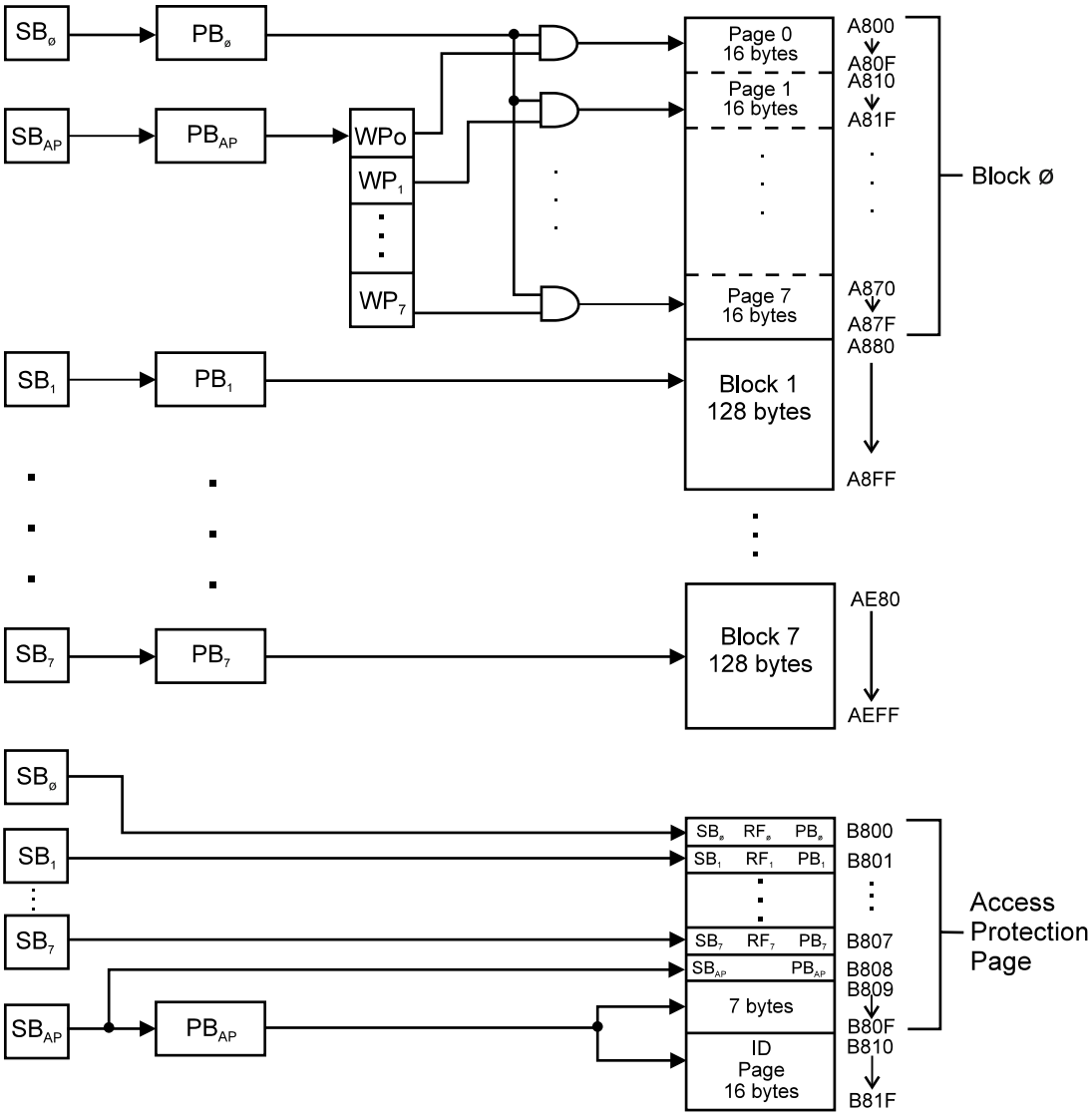
The AT24RF08C provides a mechanism to divide block 0 into eight 128-bit (16 byte) pages that can be individually protected against writes from either port. These eight write protection (WP) bits are stored within a byte of the access protection page and are organized such that the LSB protects the first 128 bits and so on. If a bit in this byte is set to a one and the PB_0 field is set to 11, then writes are permitted on the page corresponding to the WP bit. If the WP bit is set to a 0 or the PB_0 is any value other than 11, then writes are not permitted in that page.

The Write Protection hierarchy for serial accesses is shown on the following page. In this drawing the bits within the boxes to the left of the arrows are the only thing that determine whether or not the bit in the box to the right of the arrow can be written. Read access control is not shown in this diagram. Addresses listed in this diagram are for the serial port assuming that the R/W bit in the command byte is set to 0.

For example, when SB1 is a 1, the PB1 field can be written to any value by the system. When the PB1 field is 11, Block 1 can be written by the system. Note that the state of the SB1 bit does not affect whether or not Block 1 can be written.

There is no individual page Write Protection for any other block other than block 0 within the device. Within the remaining blocks on the chip, access permissions are controlled on a block basis (PB or RF bits) or full chip basis (WP pin) only.

Write Protection Flow



EEPROM Tamper Latch

There is an additional EEPROM tamper latch that can be set from the RFID port and reset from the serial port of the device. Resetting this bit from the serial port takes less than 10 ms. Setting of this bit from the RFID side when powered from L1/L2, takes about 7.9 ms but requires less than 30 µA of current. See “RFID Command” on page 8.

Access to this tamper bit from the serial interface is via the LSB of the tamper byte of the access protection page. See “Access Protection Page” below. The bit can only be set to 0 via the serial port. Attempts to write it to a value of one are ignored.

Access Protection Page

The serial port may be used to read and write the Access Protection Page (APP) and ID Page using device access codes of B8 and B9 (hex) instead of the normal value of A8 through AF (hex) that are used to access the rest of the EEPROM memory. The second byte of write commands (the word address) should be in the range of 00 through 0f (hex) for the APP page and 10 through 1F (hex) for the ID page. This coding is shown below.

Reads and writes to these two pages may take place on a single byte basis only. Multi-byte operations will be NACK'ed.

As an example, the bit encoding for a single byte read and write command are shown below.

The AT24RF08C will acknowledge all device addresses of B8 or B9 (hex). If the most significant three bits of the word address are not all 0 (indicating an address outside the Access Protection and ID pages), the chip will NACK the access.

Bytes 0 through 7 of the APP contain 8 identical sets of access control fields (PBx, RFx, TWx and SBx) for each of the eight blocks of memory on the chip, which operate according to the table listed in the Access Protection section above. When the sticky bit in one of these bytes is set, that byte can be written by the system. Once a sticky bit is reset (written to zero) by the software, the byte containing it can no longer be modified by the software until the next power cycle. These bytes can always be read by the system.

Byte 8 contains another PB field (PB_{AP}) as bits 0 and 1 and an additional sticky bit (SB_{AP}) as bit 7. The value of the PB_{AP} bits controls read and write access to the last 7 bytes (#9-15) of the APP and all 16 bytes of the ID page according to the encoding listed in the "Access Protection" section above. The value of the PB_{AP} bits can only be changed (via writes from the serial port) when SB_{AP} is high. This byte can always be read by the system. Bits 0 through 6 of this byte are stored in EEPROM memory and do not change when the power is cycled or the PROT pin changes state.

Byte 9 contains the 8 block 0 write protection bits (WP) for each page within block 0.

Byte 10 is the tamper byte, and the LSB of this byte can be used to determine if the "set tamper" command had been executed from the RFID port. This bit can be reset in software via the serial port by writing a 0 to it.

Byte 10 also contains the coil detection control. This feature is intended to permit the system to determine if a coil is connected to the pins. It works by driving a small current through the coil pins and determining if there is a low resistance between them. The coil resistance must be less than R_{COIL} for the coil to be properly detected. To enable this, the Detect Enable (DE) bit should be set to a 1. After a delay of at least 200 µs, the Detect Coil (DC) bit is then read and a "1" indicates that a coil is present.

Note that the RFID interface may not function properly when the DE bit is set to a 1, and so the software should ensure that it is always written to a 0 when the coil detection sequence has completed. The DE bit is automatically reset to a 0 upon power-up or when PROT is held low, but is not timed out internally by the device.

When the DE bit is low, the value of the DC bit will default to a high state. This does *not* indicate the presence of a coil, as the state of the DC bit is only valid when the DE bit is high.

Bytes 11 through 14 are currently reserved and should not be used by the system. Byte 14 may not be written by the device (via either interface) at any time.

Access Protection Page Examples

For Write Operations:

1 0 1 1 1 0 0 0 0 0 0 A_4 A_3 A_2 A_1 A_0 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0

For Read Operations:

1 0 1 1 1 0 0 1 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0

Byte 15 contains device revision information. It is set at the wafer production facility and cannot be changed in the field, so any write to this byte will be ignored. The least significant three bits are used to show the production revision for the part. The next three bits are used to denote the option set chosen and the most significant two bits describe the basic functionality of the device. The value of this byte is 01 001 001, or 49 (hex).

The memory map for the access protection page is shown in the table below. In this table, an x means that the value is a don't care upon writing and that it is undefined upon reading. The RF and PB fields are all two bits wide, and the Device Revision field is 8 bits wide. All other fields are one bit wide.

APP Memory Map

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	SB_0	TW_0	RF_0		x	x	PB_0	
1	SB_1	TW_1	RF_1		x	x	PB_1	
2	SB_2	TW_2	RF_2		x	x	PB_2	
3	SB_3	TW_3	RF_3		x	x	PB_3	
4	SB_4	TW_4	RF_4		x	x	PB_4	
5	SB_5	TW_5	RF_5		x	x	PB_5	
6	SB_6	TW_6	RF_6		x	x	PB_6	
7	SB_7	TW_7	RF_7		x	x	PB_7	
8	SB_{AP}	x	x	x	x	x	PB_{AP}	
9	WP7	WP6	WP5	WP4	WP3	WP2	WP1	WP0
10	DE	DC	x	x	x	x	x	Tamper
11	*reserved*							
12	*reserved*							
13	*reserved*							
14	*reserved*							
15	Device Revision							

With the exception of the 9 sticky bits (SB) and the two coil detect bits (DE and DC), all bits within the Access Protection Page are stored in EEPROM memory. Their state does not change if power is removed or when the PROT pin is held low.

The following page of memory (accessed with A_4 = 1) contains the ID field transmitted by the device from the RFID port. Bytes within it are accessed via a device address byte of B8 / B9 (write / read, hex) and a byte address of 10 through 1F (hex). Reading and writing to this ID page is permitted when PB_{AP} is 11. The least significant three bits of the first byte should vary to optimize multiple tag performance.

The MSB of the last byte of the ID page is a lock bit that controls writes to the ID page from the RFID port. If this bit is a 0, writes to this page from the RFID part are locked out (prohibited). This bit does not affect operation from the serial side, and can be read and written to either state normally from the serial port. The ID page can always be read from the RFID port.

Please note that neither the RF fields nor the TW bits protect the ID page against writes from the RFID port. Unless the ID value is locked using the ID lock bit, the user can write to the ID page regardless of the state of any access control bits.

Other than setting the tamper bit via the RFID commands or reading the ID field when so directed, there is no way for the RFID port to directly read or write the access protection page.

Serial EEPROM Exceptions

In general, the two-wire serial interface on the AT24RF08C functions identically to the AT24C08. The following exceptions exist, as noted elsewhere within this document.

- Pins 1, 2 and 3 have a different usage.
- Access to various blocks may be restricted via the access protection circuitry.
- The two block address bits (B2 and B1) in the command byte are ignored with all read commands. They are set only via the write command.
- Multi-byte reads do not cross block boundaries, but instead wrap to the beginning of the block.
- Operation of the serial bus at 400 kHz is not guaranteed.
- Maximum operating voltage is 5.5V, maximum operating temperature is 85×C.
- The serial port will be reset whenever the PROT pin is low.
- If a multi byte read is in progress when an RFID write starts, all data will be read as all 1s.
- Under some circumstances, subsequent bytes within a multi-byte read may have their data returned as all 1s to the serial port if a read is simultaneously requested from the RFID port.
- If more than 16 bytes are written to the EEPROM with a page write, overlapping bytes will have their values corrupted.
- If V_{CC} is 0V, the device draws current on the SDA, SCL, WP and PROT pins when they are brought above 0V.

RFID Port Operation

The AT24RF08C includes a powerful and flexible RFID communications port that permits moving data into or out of the device through a simple coil antenna. Features include automatic serial number transmission as well as commands for explicit reads and writes to specified locations within the EEPROM. Special capability has been added to permit a tag to be individually identified and selected when it is within the field at the same time as the other tags.

The general strategy for implementing multiple tags within the field is as follows:

Upon power-up, the tag waits a random period of time and then transmits, as a header, a fixed pattern that occupies four bit times. The value of each half-bit time is fixed at the pattern 01 11 11 10. (this is interpreted as one half-bit time with no modulation, 3-bit times of modulation and another half-bit time of no modulation).

Within the following listening window, the tag must receive an acknowledge pulse from the reader. See the “Listening Window” section for restrictions on this transmission.

If the tag does not see an acknowledge pulse during the specific time within the listening window, but sees an acknowledge pulse or command issued by the reader to another tag, it goes into an infinite listening window until the other tag is complete with its transaction.

If the tag does not see an acknowledge pulse or command from the reader at any time, it will wait for a random length of time before transmitting its four bit header again.

If it does receive this acknowledge pulse during the specific time, then it will continuously transmit its complete ID (defined below) with a three bit listening window between frames, until a command is received from the reader.

After the ID has been properly received by the reader, the tag will expect to receive a command from the reader during the three bit listening window between ID frames. One possible command is to set the QUIET bit, causing the device to remain idle until the next power down or global command. Remaining tags will then follow the same procedure until each has its QUIET bit set.

ID Configuration

After the chip’s header field has been acknowledged, the chip will transmit as its ID number, the first 12 EEPROM bytes in the ID page, starting with byte 0. This transmission will start 1664 ms after the end of the header transmission. See “RFID Acknowledge Timing” on page 16.

This ID transmission will be preceded by a single start bit that has a logical value of 1, and terminated by a single stop bit that has a logical value of ‘0’. These start and stop bits bracket each page or block of data transmitted by the device as a result of a read or write command.

After transmission of the ID frame, the device will delay transmission during a 3 bit listening window to listen for a command to be initiated before repeating the ID transmission again. Commands sent to selected tags must be initiated during the t_{CDM1} interval within this listening window, as per the “Listening Window” section on page 9.

If a write is taking place to the EEPROM from the serial port, the device will transmit to the reader a logical 0 in place of the ID value until that write completes. If a write from the serial port has started before the command is issued by the reader, then the command will be aborted and the 4 bit header sent. If a serial port write starts after a read command has commenced, then a 0 will be transmitted to the reader during the time that the EEPROM is busy with the write. In some cases, reads from the serial port will also cause data to temporarily be read as 0’s.

Non EEPROM aspects of the RFID port operation, including setting of the tamper bit, will take place normally regardless of the actions on the serial port. Operation of the RFID port does not depend on the state of any pin or the state of any sticky bits, as power to the chip may not be applied via the VCC pin when such operations are taking place.

RFID Commands

The explicit commands implemented in this tag permit the reader/writer to directly access individual areas within the memory array and are encoded as follows. In all cases below, "C_1 C_0" represents the two bit error detection field (see "Error Detection" on page 11) for the command that is used to prevent improper command execution.

For all commands, the first three bits transmitted (b_{10} - b_8) form a three bit unique command initiation pattern (CIP) that allows the transponder to be synchronized with the reader / writer. The middle bit of this pattern (signified by 'e' for error in the table below) is an entire bit time of no modulation, which is a Manchester error. The entire command initiation pattern consists of ½ bit time of modulation followed by two bit times of no modulation followed by ½ bit time of modulation.

Command Encoding

b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	Meaning
0	e	1	B_2	B_1	B_0	0	0	0	C_1	C_0	Set Block Address Latch (BL) to B
0	e	1	P_2	P_1	P_0	0	1	0	C_1	C_0	Set Page Address Latch (PL) to P
0	e	1	1	1	1	1	0	0	C_1	C_0	Set Block Address Latch (BL) to ID Block
0	e	1	P_2	P_1	P_0	1	0	1	C_1	C_0	Write Page P in Block BL (followed by 128 bits of data)
0	e	1	P_2	P_1	P_0	0	0	1	C_1	C_0	Read Page P in Block BL (followed by 128 bits of data)
0	e	1	W_1	W_0	0	1	1	1	C_1	C_0	Write Word W, Page PL, Block BL (32 bits of data)
0	e	1	W_1	W_0	0	0	1	1	C_1	C_0	Read Word W, Page PL, Block BL (32 bits of data)
0	e	1	0	1	0	1	1	0	C_1	C_0	Disable Chip Until Power Down (set QUIET bit)
0	e	1	1	0	1	1	1	0	C_1	C_0	Global Reset QUIET bit
0	e	1	1	1	0	1	1	0	C_1	C_0	Set EEPROM Tamper Latch (selected tag only)
0	e	1	1	0	0	1	1	0	C_1	C_0	Global Set EEPROM Tamper Latch
0	e	1	W_1	W_0	1	1	1	1	C_1	C_0	Global Write Word W, Page 1, Block 0 (32 bits of data)

The three global commands may be sent to **selected** chips during the second bit of any three bit listening window or to **unselected**, chips in the **init** state or **quiet** chips at any time. In general, they operate upon all tags within the field, however, if a chip is currently transmitting data to the reader or waiting for an ACK pulse, it will not be able to recognize these commands.

For the Read and Write commands, the data corresponding to the accessed word or page is repeatedly transmitted back to the reader by the device, after the command has completed. This permits a verify function for the write operation and a repetition check for the read data.

After the last bit of a read command is sent, there is a delay of 136 cycles before the first read data bit is transmitted by the chip. After a write command, there is a delay of t_{wd} before the written data is transmitted back to the reader. There should be no modulation of the carrier by the reader during these delays.

Between each 32 or 128 bits of data transmitted, there is a 3-bit listening window to synchronize the reader and/or to permit the reader to issue a new command to the device. See "Listening Window Structure" on page 9.

There is no delay interval between the transmission of the write commands and the data that is to be written. Immediately after the last bit of the command (C_0), the most significant bit of the data should be sent to the device without any interruption.

There is no retransmission of the data after the Global Write Word command, since multiple tags are expected to be able to have executed this command at the same time. To verify proper operation of this command, each tag must be individually selected and the word read explicitly using the Read Word command.

Both the BL and PL registers used in the read and write commands to determine the address are set to 0 upon power-up. The PL value is automatically set to the transmitted value when the Write Page and/or Read Page commands are executed.

The “Set BL to ID” command permits the ID page (page 1) to be written from the RFID port if the lock bit is set to a one. This lock bit is the 121st bit sent as part of a write page command or the 25th bit sent as part of a write word 3 command. The first 96 bits of this page are the ID bits which are transmitted by the chip in the same order as they are written.

The PL register value is ignored when the BL points to the ID page. Also, the page number is ignored on page write commands.

Listening Window Structure

After any header, ID or data element is read from the device (for any reason) the chip delays further transmissions for a period of time to determine if the reader intends to communicate with the tag. The length of the various delays and the actions that the device takes during this delay depends on the current state of the device and/or any command issued by the reader.

In general, the tag expects to see communications from the reader start between the middle of the first bit time and the end of the second time (256 µs to 1024 µs) after the end of the previous communication. The beginning of the first and the entire third write bit times are ignored in order to prevent the tag from erroneously seeing its own modulation as incoming from the reader. Specific timing requirements for these communications are shown in the RFID Acknowledge timing diagram and the RFID Command/Data Timing Diagram on page 16.

There are four states possible for tags that are sufficiently in the field for the internal voltage to be above the reset level. They are listed below and shown in bold throughout this document.

Init
Upon power up, and after execution of the global reset quiet bit command, all chips are in this state. Chips that do not have their QUIET bit set also go into this state after the execution of a Disable/Set Quiet command. While in this state, chips delay a random length of time and then transmit their 4-bit header. Tags in this state honor all global commands except those that start during the period in which they are transmitting their header and during the first 512 µs of the listening window. They transition to **Unselected** after global command execution, other than global reset quiet which stays in init.

Selected
If the reader issues an acknowledge pulse to a tag in the **init** state during the second write bit time after the header is transmitted, then the tag is **selected** and it will repeatedly transmit its ID until the reader sends a command to the tag. The tag remains **selected** through the entire sequence of ID transmission and subsequent command execution unless there is a fault of some kind.

Unselected
If a tag in the **init** state senses modulation interval greater than 32 µs in length during any bit time other than the second then it moves into the **unselected** state, and remains that way until it sees a Disable Chip command. **Unselected** tags also honor the three global commands while they are “waiting”. All other commands are ignored.

Quiet
When in the **quiet** state, the chip does not activate its modulation resistor at any time. Only the three global commands will be honored by the chip. All other commands are ignored.

The following paragraphs describe five kinds of delays that are possible.

Random
The chip delays a pseudo random length of time. The length of this delay sequences through the following number of read bit times (128 µs each): 64, 48, 24, 32, 56, 40 and 72. The starting point among this list is based on the first three bits of byte 0 of the ID page within the EEPROM. If these bits are 111, then the sequence above will be preceded by a 16-bit delay. The minimum and maximum delays are 2048 µs and 9216 µs, respectively.

Three Bit
The device waits for three write bit times and then one read bit time (for a total of 1664 µs) before retransmitting the data that was just transmitted. During the t_{CDM1} interval, the reader may issue a command to the chip. See “RFID Command/Data Timing” on page 16.

Long
After certain commands, **selected** chips wait indefinitely for the next command from the reader. This command should start during the t_{CDM1} interval after the end of the command transmission.

Infinite
Unselected chips wait in this state for any of the three global commands or the Disable Chip command. If no legal command transmission ever occurs, then the device will stay in this delay loop for as long as power is applied from the RFID port.

Quiet
Similar to “infinite” except that only the global commands are honored. If the operation of the system includes only multi tag ID transmission along with the use of the global set tamper command, it is useful to note that the global set tamper command should be sent to every device before the Disable Chip/Set Quiet command is sent to the **selected** tag. Since tags in the **init** state transition to **unselected** with a global command, the Disable Chip/Set Quiet will automatically bring them back to **init** to complete the multi-tag discrimination procedure. In some cases, it is possible for multiple tags to be **selected** inadvertently, or for tags to be in a state that the reader does not expect. Normally, a Global Reset Quiet command may be issued to reset all tags, but this will be ignored by a device while it is transmitting its ID. Issuing this command three times in succession will ensure that any rogue chips go back to the **init** state.

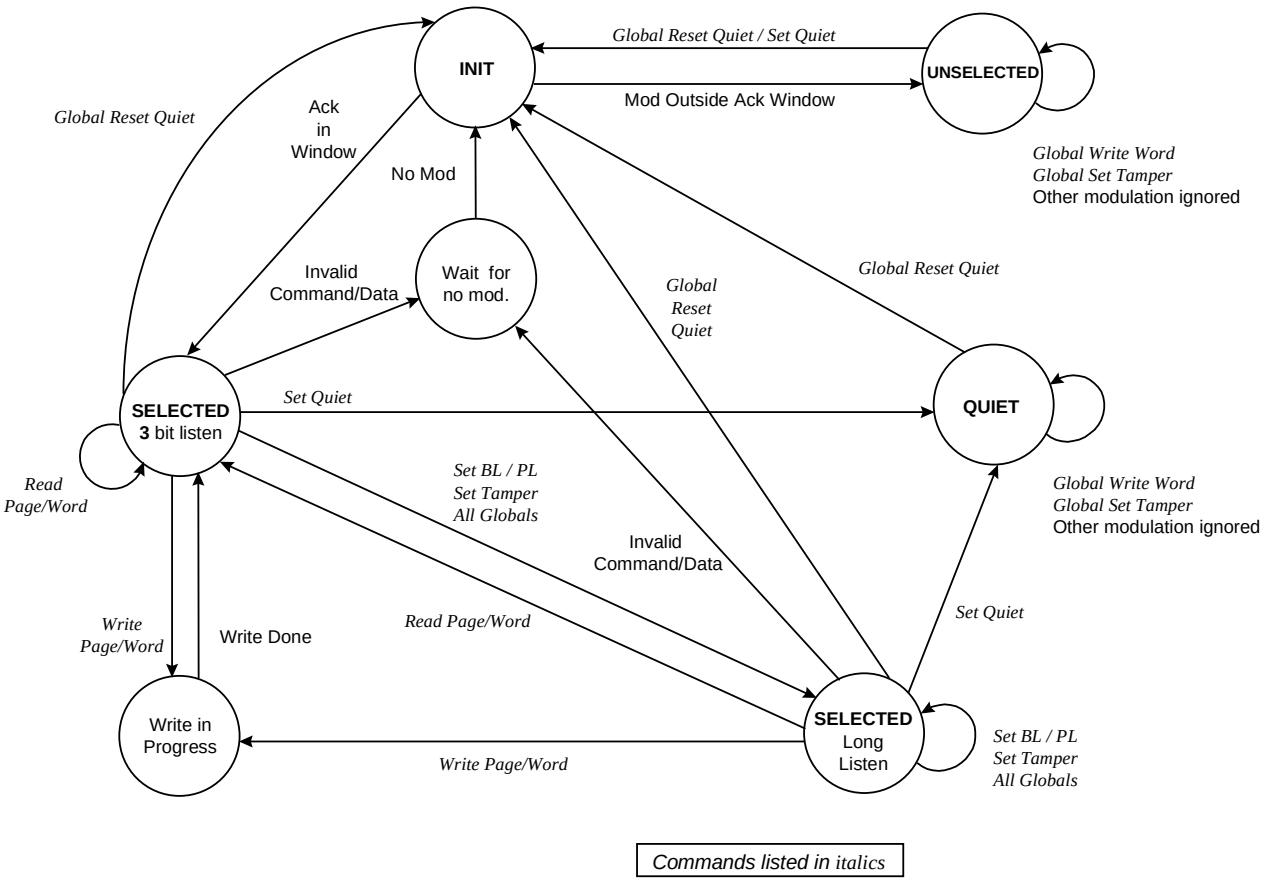
The table below combines the two lists above to show what delay is used, depending on the current state of the chip and the command that is issued by the reader. In the State Transition Diagram, shown on the next page, the same information is shown graphically in a state diagram for the chip.

Delay Length for Commands

Command	Selected	Unselected	Quiet
Set Block Address Latch	Long	Infinite	Quiet
Set Page Address Latch	Long	Infinite	Quiet
Write Page P in Block BL	Three (1)	Infinite	Quiet
Read Page P in Block BL	Three	Infinite	Quiet
Write Word W, Page PL	Three (1)	Infinite	Quiet
Read Word W, Page PL	Three	Infinite	Quiet
Global Write Word W	Long	Infinite	Quiet
Set EEPROM Tamper Latch	Long(1)	Infinite	Quiet
Global Set Tamper Latch	Long	Infinite	Quiet
Disable Chip/Set QUIET bit	Quiet	Random	Quiet
Global Reset QUIET bit	Random	Random	Random

Note: 1. After the data for a write is sent to the device, there will be a delay of T_{WD} or T_{TWD}. The written data will be read back to the reader and then the ‘three bit’ window will occur. During this delay, the device ignores all data sent to it.

State Transition Diagram



Error Detection

In order to increase the reliability of data transmissions to the AT24RF08C, an error detection field must be sent by the reader after the command word and each byte of data sent from the reader. This field is computed as the number of bits turned on in the byte modulo 4. In order to prevent the checksum from matching the data for repeated 0's or 1's, the least significant bit (c_0) is then inverted. For the command word, only the 6 varying bits (b_7 - b_2) are used to compute the checksum.

There are several levels of error detection utilized to prevent improper execution of a command. If the command encoding is illegal, or the checksum is wrong, or if there is a Manchester error in either the command or data or if there is a protection failure, then the entire command will be aborted. Once in that state, the device will wait a random period of time before transmitting the header sequence.

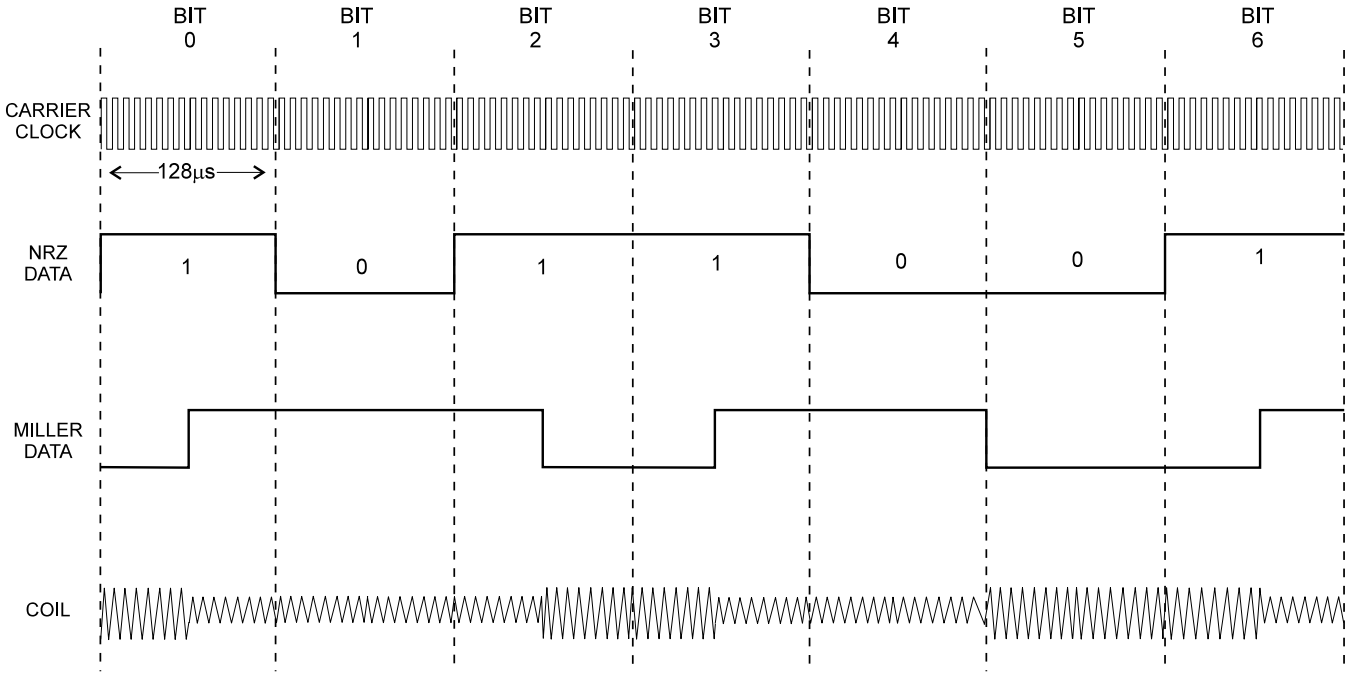
On both ID and data sent from the chip, the chip generates and transmits a single parity bit after each 8 data bits are sent to the reader. Internally, parity is computed in such a way that the number of 1s in each 9 bit group is even. The start and stop bits are not included in the parity generation. No parity is generated on the 4-bit header. It is expected that the reader may either embed additional error detection bits within the data and/or read the data two or more times to reduce the rate of bit errors.

Transmission: Encoding and Modulation

Data is transmitted to the reader using resistive modulation which is implemented as a variable modulation resistor switched across the coil pins. Data from the EEPROM is encoded using Miller Encoding before driving the modulation resistor. If the output of the Miller Encoder is a 1, then the modulator resistor is turned on and vice versa. In Miller Encoding, if the data state is a 1, there is a transition in the middle of the bit time. If the data state is a 0, there is no transition if the next data bit is a 1 or a transition at the end of the bit time if the next data state is a 0.

Each data or ID group transmitted (other than the header) includes a start bit which has a value of 1. This is always interpreted as a transition from modulator-off to modulator-on in the middle of the start bit time, preventing a half-bit time modulation pulse. Data is transmitted from the chip at a rate of one bit (into the encoder) for each 16 carrier cycles. After the data has been transmitted, a single stop bit having the value of 0 will be transmitted. Depending on the state of the last parity bit, this will be either one cycle of modulation or one cycle of no modulation. The following diagram shows the functional signal waveforms for data transmission.

Data Transmission



Reception: Decoding and Demodulation

For data received by the chip, a drop in amplitude is interpreted as a low state, while an increase in amplitude indicates a high state. The output of this demodulator is inverted and then decoded using Manchester decoding before being interpreted as commands or data.

In Manchester decoding, (sometimes called BiPhase), there is a transition in the middle of each bit time. If this is a high-to-low, the data state is a 0, and if low-to-high a 1. Data is received by the chip at a rate of one bit (out of the decoder) for each 64 carrier cycles.

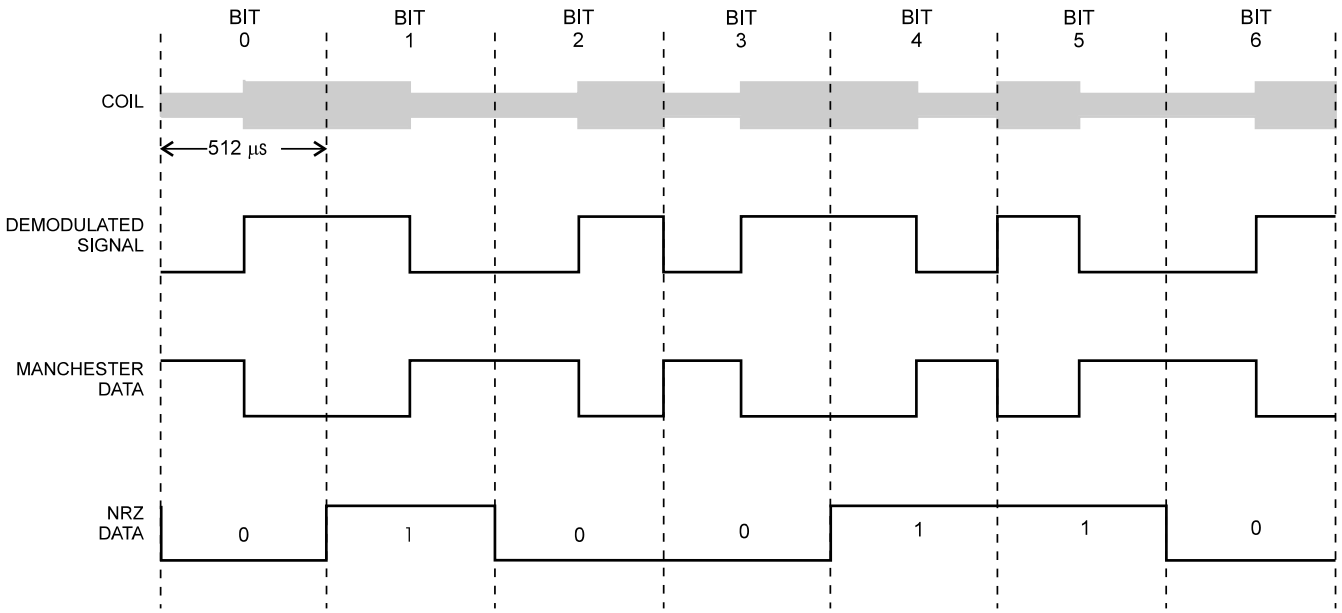
Each command must be preceded by a command initiation pattern (CIP). The receiver uses the leading edge of the first modulation change of the CIP to automatically synchronize to the incoming data stream. That edge must occur during the t_{CMD1} interval after the end of the last bit previously transmitted or received by the chip. This edge is used to start a bit clock against which all remaining edges are timed.

The remaining two edges within the CIP occur during the middle of the first and third bit times of the command. They must occur within specific time intervals (t_{CMD2}) from the beginning of the bit time, and their specific time locations (within the bit times) are used to synchronize with subsequent edges (t_{CMD3}) occurring in the same direction (rising or falling). Edges that correspond to Manchester changes at the beginning/end of a bit are not explicitly used by the chip.

If no edges of the CIP fall within the t_{CMD1} window after a read of some sort (including ID read), the chip will retransmit the data that was previously read.

The following diagram shows functional waveforms for data reception.

Data Reception



Voltage Levels

The chip includes a voltage reference to ensure that command initiated reads and writes from the RFID port are only performed when the power supply voltage on the chip is above the level (Vcoil2) at which EEPROM reads and writes can be guaranteed. If an EEPROM read or write is attempted when the voltage is too low, the command will be aborted.

Below the Vcoil2 level, but above a minimal operating voltage level of Vcoil1, header and ID reads are permitted. In addition, the two tamper latch commands and the two QUIET bit commands may also be executed at lower voltages. Because the EEPROM data may not be read correctly at this voltage, the ID field must contain some error detection information stored within it.

Proper setting of the tamper bit feature is guaranteed only if V_{COIL} is above 3.7V for greater than 6.1 ms, but under typical conditions, the circuit will operate over a much wider range.

When power is removed from the serial interface side (VCC pin), the RFID operation will be momentarily reset while the internal circuitry switches the internal power supply to the RFID bridge. When the voltage on the VCC pin is held to above 0.6V but less than 2.4V (both nominal), all read and write commands from the RFID port may be inhibited. ID transmission and tamper bit commands may be executed, although their operation may not be correct.

Absolute Maximum Ratings

Coil Voltage (peak-to-peak) Maximum	24V
Operating Junction Temperature	-40 to +85°C
Storage Temperature (Without Bias)	-55 to +125°C
Voltage on V_{CC} with Respect to Ground	6.0V
Voltage on SDA, SCL, PROT and WP	-0.1 to V_{CC} +0.3V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

Parametric Specifications

Unless otherwise noted, all specifications are over the temperature range of -40°C to +85°C.

RFID DC Specifications(1)

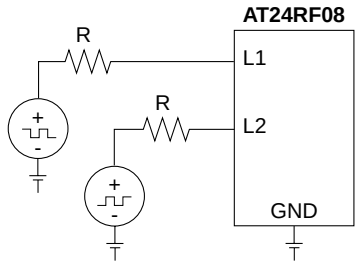
At f_{COIL} = 125 kHz, V_{CC} (SERIAL) = 0V.

Name	Min	Typ	Max	Units	Notes
P_{COIL}			160	mW	Maximum Power Dissipation from L1/L2, Peak
V_{COIL1}	1.6	2.2	3.1	V	Coil Voltage(2) for ID Transmission
V_{COIL2}	2.7	3.0	3.7		Coil Voltage(2) for EEPROM Writes and Reads
I_{L1-L2}			20	mA	Peak Clamp Current
I_{CCR}		7	10	µA	During EEPROM Read, $V_{L1/L2}$ = 2.2V
I_{CCT}		25	30	µA	During Tamper Bit Write, $V_{L1/L2}$ = 2.2V
I_{CCW}		150	200	µA	During EEPROM Write, $V_{L1/L2}$ = 3.0
V_{CNF}	5.0		7.0	V	10V Through 400 Ω, Prior to Header
V_{MNF}			4.0	V	10V Through 400 Ω, During Header
V_{CFF}	4.0			V	4.5V Through 5K Ω, Prior to Header
V_{MFF}			3.4	V	4.5V Through 5K Ω, during header
DV_{RCV}	1.0			V	Modulation Voltage Delta During Reception
C_L			5	pF	Input capacitance on L1/L2 at 5V, Not Tested
R_{COIL}			950	Ω	Maximum Coil Resistence for Coil Detection

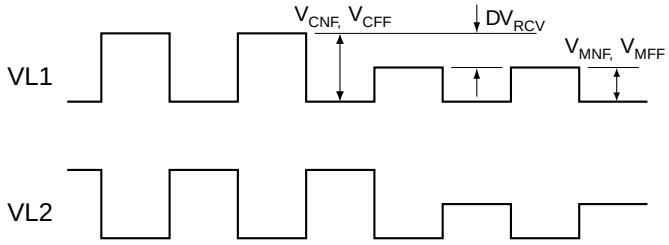
Notes: 1. Some parametric limits are design targets that may be refined on the basis of production history.

2. Coil voltages are measured with respect to the on chip ground, which is centered on the AC voltage from the coil. Peak-to-peak coil voltages would be double those listed above.

Transmit Test Circuit



Test Waveform

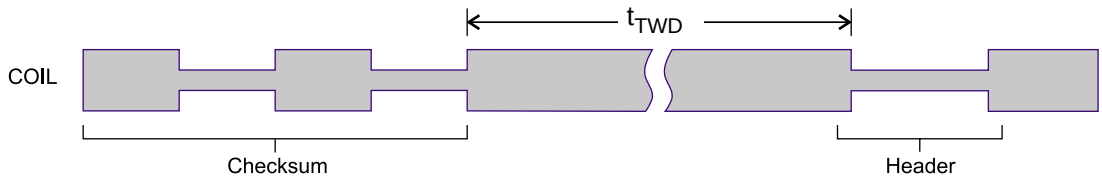


RFID AC Specifications

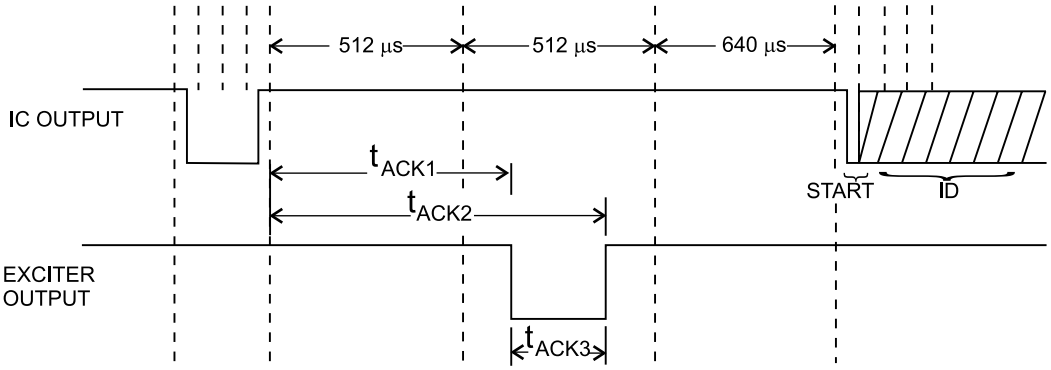
At f_{COIL} = 125 kHz, except where noted.

Name	Min	Typ	Max	Units	Notes
f_{RF}	120	125	130	kHz	Coil Excitation Frequency
t_{BITR}	123	128	133	µs	Read Bit Time, Over f_{RF} Range
t_{BITW}	493	512	531	µs	Write Bit Time, Over f_{RF} Range
t_{WD}	5.9		11.8	ms	Write Delay, Modulation Edge to Modulation Edge
t_{TWD}	5.6	7.9	11.8	ms	Tamper Bit Write Delay, Modulation Edge to Modulation Edge
t_{MODF}		16	32	µs	Input Modulation Fall Time, L1 or L2, Not Tested
t_{MODR}		16	32	µs	Input Modulation Rise Time, L1 or L2, Not Tested

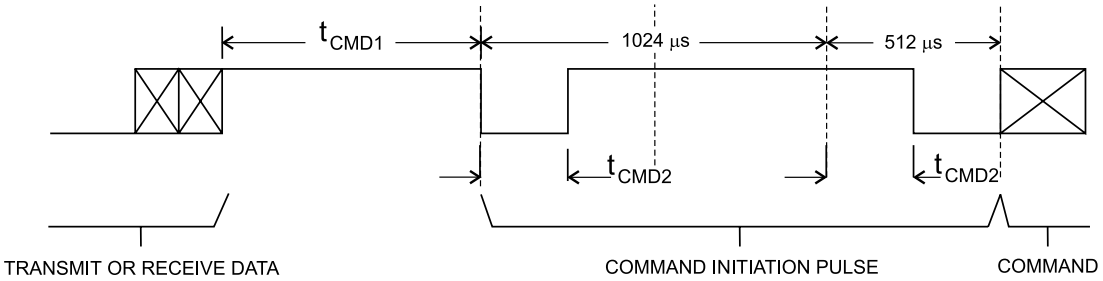
RF Write Delay

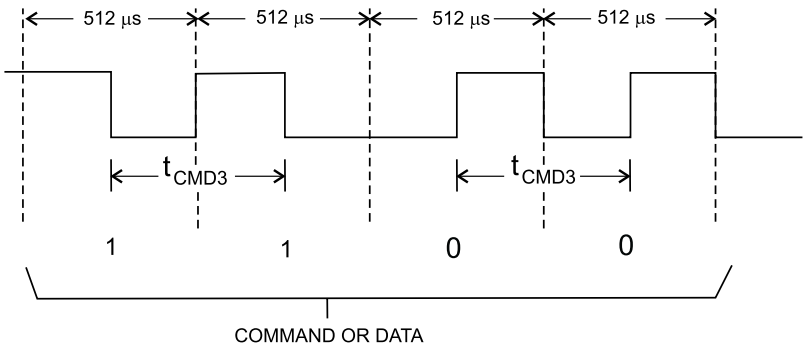


RFID Acknowledge Timing



RFID Command/Data Timing



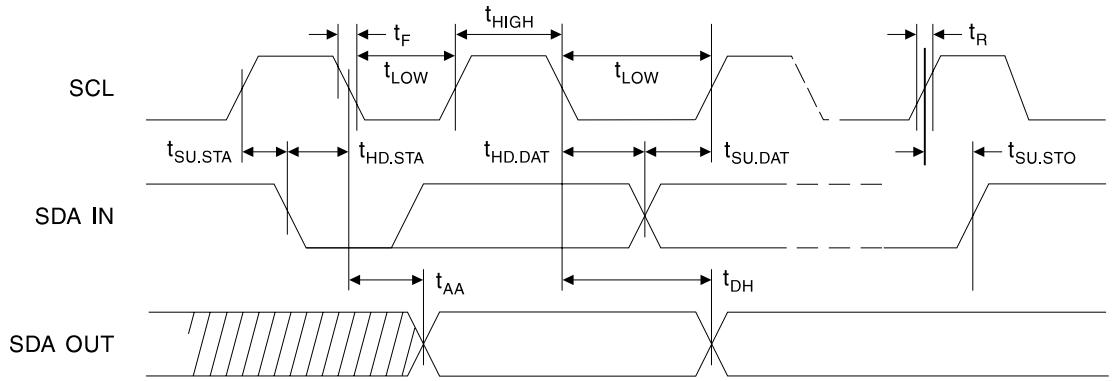


RFID Protocol AC Specifications

At f_{COIL} = 125 kHz.

Name	Min	Typ	Max	Units	Notes
t_{ACK1}	256	640	896	µs	Delay from Header End to ACK. Start
t_{ACK2}	640	896	1024	µs	Delay from Header End to ACK. End
t_{ACK3}	32	256	512	µs	Acknowledge Pulse Width
t_{CMD1}	256	768	1024	µs	Delay from Data End to CIP Start
t_{CMD2}	32	256	368	µs	Delay from Bit Time Start to Modulation Change
t_{CMD3}	400	512	624	µs	Delay from Modulation Change to Next Same Change

Timing Diagram for Serial Interface AC Specifications



Serial Interface AC Specifications

C_L = 1 TTL Gate and 100pF, except as noted. VCC = 2.4V to 5.5V.

Name	Min	Max	Units	Notes
f_{SCL}		100	kHz	Clock (SCL) Frequency
t_{LOW}	4.7		µs	Clock (SCL) Pulse Low-width
t_{HIGH}	4.0		µs	Clock (SCL) Pulse High-width
t_I		100	ns	Noise Suppression, Not Tested
t_{AA}	0.1	4.5	µs	Clock low to Data out Valid
t_{BUF}	4.7		µs	Bus Free before Transmission, Not Tested
$t_{HD.STA}$	4.0		µs	Start Hold Time
$t_{SU.STA}$	4.7		µs	Start Set-up Time
$t_{HD.DAT}$	0		µs	Data In Hold Time
$t_{SU.DAT}$	200		ns	Data In set-up Time
t_R		1.0	µs	Inputs Rise Time, Not Tested
t_F		300	ns	Inputs Fall Time, Not Tested
$t_{SU.STO}$	4.7		µs	Stop Set-up Time
t_{DH}	300		ns	Data Out Hold Time
t_{WR}		10	ms	Write Cycle Time, EEPROM or Tamper Write

Serial Interface DC Specifications

Name	Min	Typ	Max	Units	Notes
V_{CC}	2.4		5.5	V	Operating Voltage, V_{CC} pin
I_{CCR}		50	100	µA	At V_{CC} = 5V, f_{SDA} = 100 kHz, EEPROM Reads
I_{CCW}		0.5	1.0	mA	At V_{CC} = 5V, f_{SDA} = 100 kHz, EEPROM Writes
I_{SB1}		8	12	µA	At V_{CC} = 5.5V, SDA, SCL = V_{SS}, RFID Idle
I_{SB2}		6	8	µA	At V_{CC} = 3.3V, SDA, SCL = V_{SS}, RFID Idle
I_{LIO}		0.1	3.0	µA	PROT, SDA, SCL. V_{IN} = V_{CC} or V_{SS}
I_{LWP}			20	µA	Input Current on WP, at V_{WP} = V_{DD} = 5.5V
V_{IL}	-0.1		V_{CC} x 0.3	V	
V_{IH}	V_{CC} x 0.7		V_{CC}	V	
V_{OL}			0.4	V	I_{OL} = 2.1mA
C_I			6	pF	SCL, PROT, WP. Not Tested
C_{IO}			8	pF	SDA. Not Tested

Note: Those specifications noted “not tested” denote parameters that are characterized and not 100% tested.

EEPROM Memory

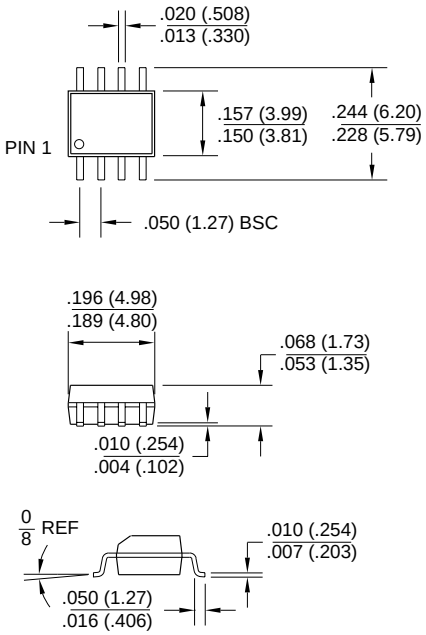
Name	Min	Typ	Max	Units	Notes
Retention	10			years	Data retention at operating temperature
Endurance	100,000			cycles	Per byte

Ordering Information

Package	Package Mark	Ordering Code
8S1	24RF08CN	AT24RF08CN - 10SC

Packaging Information

8S1, 8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC) Dimensions in Millimeters and (Inches)



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